ABSTRACT OF THE DISCLOSURE

A system and method for enabling concurrent usage of non-volatile memory for code execution and data storage/processing, comprising a hardware mechanism that can support automatic suspend and resume operations. This mechanism entails the integration of a suspend logic circuit and a resume logic circuit into the chip hardware, or the stationing of the logic chip in any way that it can operate together with the chip. This system and method enable a Flash memory chip to process code execution while it is processing erase/program operations, avoiding conflicts that ordinarily crash such a system. This is achieved by sensing the operation status of the chip and the CPU/Bus activity, and commanding the flash memory device to suspend and/or resume program/erase operations at appropriate times, so as not to conflict with read requests.